

2
3 **Design of Common-Source/Drain Active Balun**
4 **Using 90nm CMOS Technology**
5
6
7
8

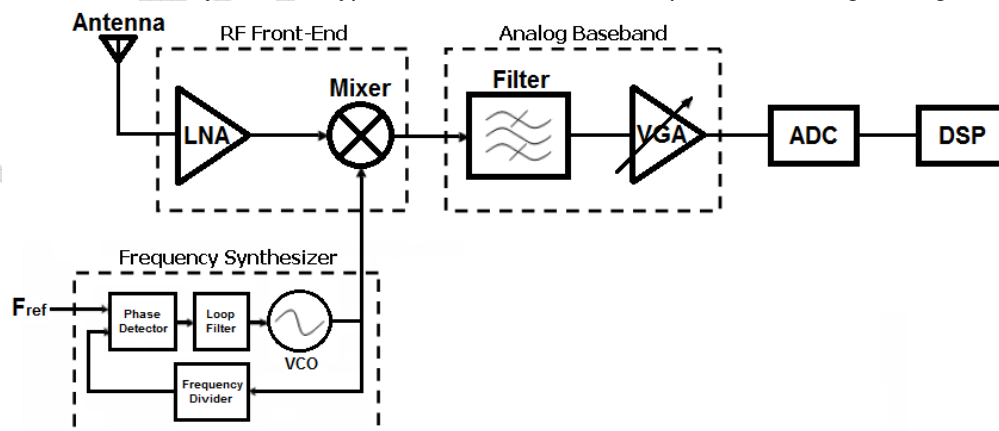
9
10 **ABSTRACT**
11

This research paper presents a design and study of a common-source/drain active balun circuit implemented in a standard 90-nm complementary metal-oxide semiconductor (CMOS) technology. The active balun design is intended for worldwide interoperability for microwave access (WiMAX) application, with operating frequency of 5.8GHz and supply voltage of 1V. Measurements are taken for parameters namely gain difference, phase difference, and noise figure. The common-source active balun design achieved a minimal gain difference of 0.016dB, phase difference of $180^\circ \pm 7.1^\circ$, and noise figure of 7.42-9.85dB, which are comparable to past active balun designs and researches. The design eventually achieved a low power consumption of 2.56mW.

12
13 *Keywords: Common-source/drain active balun; 90nm CMOS; balun; gain; gain difference,*
14 *phase difference, noise figure; WiMAX*
15

16
17 **1. INTRODUCTION**
18

19 A considerable growth of interest in technologies that could deliver higher data rates over
20 wider coverage led to the evolution of new wireless standards such as the IEEE 802.16-
21 based WiMAX or the worldwide interoperability for microwave access. Like WiMAX, other
22 communication systems namely Bluetooth, Wireless Fidelity (WiFi), and Long-Term
23 Evolution (LTE) have the radio frequency (RF) receiver front-end that proves to be a critical
24 part in the wireless system. A typical wireless receiver is represented in Fig. 1 diagram.

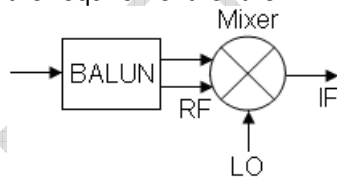


25
26 **Fig. 1. Block diagram of a wireless receiver**
27

28 Some of RF front-end circuits are often designed as differential circuits. Fully-differential
29 approach is usually preferred in RFIC design due to its advantages, particularly the high
30 immunity to common-mode noises, rejection to parasitic couplings, and increased dynamic
31 range [1-2]. In order to supply input signal to differential circuits, a building block capable of
32 supplying balanced differential signals is needed without sacrificing the performance of the
33 overall system in terms of gain, noise figure, and linearity. Active balun (balanced-
34 unbalanced) is capable to perform the necessary tasks.
35

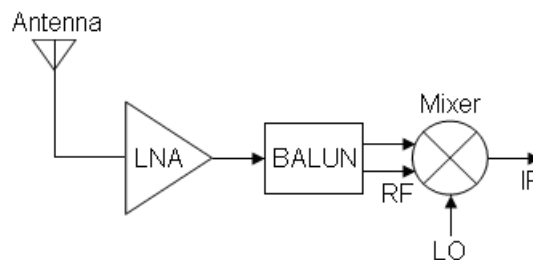
36 A balun circuit is a type of transformer that converts signals that are single-ended or
37 unbalanced with respect to ground into signals that are differential or balanced with respect
38 to ground, and vice versa. Baluns can be classified as either active or passive baluns
39 depending on the devices used. Active baluns, although unidirectional and more complex to
40 implement, are preferred over their passive counterparts because they can produce gain,
41 occupy less chip area and can operate at higher frequencies [2-3].
42

43 Active balun circuit can be used as the first block of the WiMAX receiver front-end to supply
44 differential signal to a differential low-noise amplifier (LNA). It can also be used to supply
45 differential signal to a mixer in Fig. 2. Fig. 3 illustrates the active balun circuit as an
46 intermediate block between the LNA and the mixer. Note that the configuration depends on
47 the gain, noise figure (NF), and linearity requirements of the system. Since LNA is the first
48 block in the receiver front end, it is critically designed with high gain of at least 25dB and
49 noise figure of less than 2dB. Based on past researches, active balun has relatively high
50 noise figure and lower gain performance compared to LNA, hence cannot be considered as
51 the first block in the receiver front-end. Finally, the challenge is to design an active balun as
52 an intermediate block to allow the LNA's output to connect with a differential mixer's input,
53 with performance conforming to the requirement for the WiMAX receiver front-end.



54
55
56
57

Fig. 2. Active balun supplying a differential mixer



58
59
60
61
62

Fig. 3. Active balun as intermediate block between LNA and mixer

63 2. ACTIVE BALUN DESIGN

64
65 In this research paper, a common-source/drain active balun is designed and implemented in
66 a standard 90nm complementary metal-oxide semiconductor (CMOS) technology. The
67 supply voltage (VDD) for the design is set to 1V. The lengths (L) of all transistors are set to

68 100nm, which is the minimum allowed channel length for the technology used. Transistor
 69 widths (W) are carefully computed to ensure the operation of all the transistors at saturation.
 70 As mentioned earlier, the paper deals with the design of active baluns as intermediate block
 71 between LNA and mixer in the WiMAX receiver front-end. Table 1 summarizes the target
 72 specifications of the active balun design. These values are based from past active balun
 73 researches and from the summary of parameters as per WiMAX standard [4].
 74
 75

Table 1. Target specifications for the common-source/drain active balun design

Parameters	Value
Frequency	5.8GHz
Gain difference	< 1dB
Phase difference	$180^\circ \pm 10^\circ$
Noise figure	< 10dB
Power consumption	< 10mW

76
 77 Two important parameters of the active balun are the gain difference and phase difference.
 78 Gain difference is the difference of the gains from the two output nodes of the active balun
 79 while the phase difference is the difference between the phase of the non-inverting output
 80 node (RFout1) and the phase of inverting output node (RFout2) of the active balun. Another
 81 important parameter is the noise figure (NF), which is the measure of the amount signal-to-
 82 noise-ratio (SNR) degradation introduced by the circuit as seen in the output.
 83

84 The common-source/drain active balun shown in Fig. 4 is composed of a single transistor
 85 M1. The input signal is fed into the gate of the transistor. Normal operation results in an
 86 inverted output signal at RFout2 and a non-inverted signal at RFout1. Ideally, these two
 87 outputs would have the same amplitude with a phase difference of 180° . Load resistors R1
 88 and R2 determine the output voltages as well as the voltage gains of the two output signals
 89 with respect to the input signal.

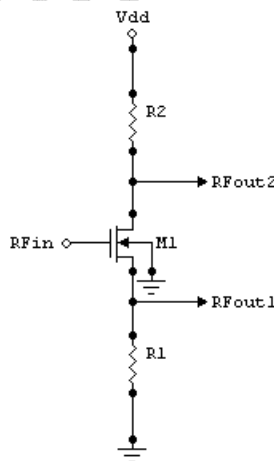


Fig. 4. Common-source/drain active balun schematic

90
 91
 92
 93
 94 Common-source topology exhibits a relatively high input impedance while providing voltage
 95 gain and requiring a minimal voltage headroom. Common-drain topology or source-follower,
 96 on the other hand, is occasionally employed as level shifters or buffers, impacting the overall
 97 frequency response. It also exhibits high input impedance. With the two topologies merged
 98 to function as an active balun, common-drain will dominate the response on the overall

99 voltage gain or attenuation because of the feedback effect of load resistor R1 with respect to
100 the input.

101

102 Common-source/drain active balun is ideal for low voltage, low power WiMAX application
103 due to low number of stacked devices. The active balun cannot actually produce gain in
104 RFout1 due to its source-follower configuration. Since the two outputs should have
105 balanced gain or attenuation, RFout2 should adjust and thus cannot produce gain. Hence,
106 one important goal for this active balun design is to minimize the attenuation in outputs
107 RFout1 and RFout2 and should be balanced with respect to the input RFin.

108

109 Drain current I_{DS} of transistor M1 is also the total supply current that is derived from the total
110 power consumption of the active balun. With supply voltage $V_{DD} = 1V$, I_{DS} could be
111 computed in Eq. (1) in terms of the output DC or bias voltages V1 (or V_{RFout1}) and V2 (or
112 V_{RFout2}) and the output loads R1 and R2.

113

$$I_{DS} = \frac{V1 - 0}{R1} = \frac{V_{DD} - V2}{R2} \rightarrow I_{DS} = \frac{V1}{R1} = \frac{1V - V2}{R2} \quad \text{Eq. (1)}$$

114 Assuming output loads R1 and R2 are equal to achieve a balanced response for V1 and V2
115 in terms of output swing, Eq. (1) would become Eq. (2).

116

$$V1 = 1V - V2 \quad \text{Eq. (2)}$$

117 From the expression in Eq. (1), increasing I_{DS} increases the output voltage V1, while output
118 voltage V2 decreases with I_{DS} . To achieve the minimum attenuation, V1 and V2 should take
119 into account the drain-to-source voltage V_{DS} of transistor M1. This will also maximize the
120 output swing in RFout1 and RFout2. Ensuring that transistor M1 operates at saturation
121 region, V_{DS} should be at least V_{DSAT} or the overdrive voltage V_{OV} . With supply voltage $V_{DD} =$
122 $1V$, overdrive voltage V_{OV} set to 200mV and with the two outputs balanced, output voltage
123 swings are computed as

124

$$V_{DS} = V2 - V1 \geq V_{DSAT} \rightarrow V2 - V1 \geq 0.2V \quad \text{Eq. (3)}$$

125 Substituting V1 expression in Eq. (2) into Eq. (3),

126

$$V2 - (1V - V2) \geq 0.2V \quad \text{Eq. (4)}$$

$$V2 \geq 0.6V \rightarrow 1V > V2 \geq 0.6V \quad \text{Eq. (5)}$$

127 Output DC voltage V2 is computed to swing from 0.6V to 1V. Calculating for the output
128 swing for V1,

129

$$V2 - V1 = V_{DS,Q} \geq 0.2V \rightarrow V1 \leq V2 - 0.2V \quad \text{Eq. (6)}$$

$$V1 \leq 0.6V - 0.2V \quad \text{Eq. (7)}$$

$$V1 \leq 0.4V \rightarrow 0.4V \geq V1 > 0 \quad \text{Eq. (8)}$$

130 Output DC voltage swing for V1 is calculated to range from 0V to 0.4V. As previously
131 mentioned, V1 increases with I_{DS} while V2 decreases with I_{DS} . To maximize the output
132 swing in RFout1 and RFout2, output DC voltages V1 and V2 should have values median to
133 their output range in Eq. (8) and Eq. (5), respectively. This would also safeguard transistor
134 M1 to operate at saturation region with V_{DS} of at least 200mV, while varying I_{DS} . The
135 optimized values for output DC voltages V1 and V2 are given as

$$V1 = 0.2V \quad \text{Eq. (9)}$$

$$V2 = 0.8V \quad \text{Eq. (10)}$$

136 With threshold voltage V_t set to 400mV, VOV set to 200mV, $V1$ set to 0.2V, and $V_{DS} \geq V_{DSAT}$
 137 = V_{OV} , input bias voltage could be determined in Eq. (11) to (12).
 138

$$V_{DS} = V_{GS} - V_t \geq V_{DSAT} \quad \rightarrow \quad (V_{IN} - 0.2V) - 0.4V = 0.2V \quad \text{Eq. (11)}$$

$$V_{IN} = 0.8V \quad \text{Eq. (12)}$$

139 With input DC voltage V_{IN} set to 0.8V, it could swing from maximum 1V to 0.6V. Maximum
 140 input voltage is set to align with the supply voltage V_{DD} which is at 1V. Drain current I_{DS} of
 141 transistor M1 is also the total current that is derived from the total power consumption of the
 142 active balun. Using the square-law equation in Eq. (13), transconductance g_m could be
 143 computed in Eq. (14) to (15).
 144

$$I_D = \frac{\mu C_{ox} W}{2 L} (V_{GS} - V_t)^2 (1 + \lambda V_{DS}) \quad \text{Eq. (13)}$$

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} = \mu C_{ox} \frac{W}{L} (V_{GS} - V_t) (1 + \lambda V_{DS}) \quad \text{Eq. (14)}$$

$$g_m = \mu C_{ox} \frac{W}{L} (V_{IN} - V_t - V1) (1 + \lambda V_{DS}) \quad \text{Eq. (15)}$$

145 Substituting I_{DS} from Eq. (13) into g_m in Eq. (14), an important design parameter could be
 146 determined, which is the $gmoverId$.
 147

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} = \frac{2I_{DS}}{(V_{GS} - V_t)} = \frac{2I_{DS}}{V_{OV}} = \frac{2I_{DS}}{V^*} = \frac{2I_{DS}}{(V_{IN} - V1 - V_t)} \quad \text{Eq. (16)}$$

$$\frac{g_m}{I_{DS}} = gmoverId = \frac{2}{(V_{IN} - V_t - I_{DS}R1)} \quad \text{Eq. (17)}$$

148 Proper DC input bias should be observed to realize good efficiency in terms of $gmoverId$. It
 149 can also be observed that the $gmoverId$ is affected by the load resistance $R1$. For low power
 150 design, higher $gmoverId$ is recommended [5]. As initially assumed, VOV is set 200mV for
 151 minimum attenuation and/or maximum voltage swing in outputs $RFout1$ and $RFout2$ with
 152 respect to the input $RFin$. With this, $gmoverId$ could be estimated in Eq. (18).
 153

$$\frac{g_m}{I_{DS}} = \frac{2}{200mV} = 10V^{-1} \quad \text{Eq. (18)}$$

154 It can be noted that to maintain the efficiency for low power consumption, lowering I_{DS} would
 155 also mean lowering g_m . Transistor sizing depends on the target power consumption and
 156 likewise I_{DS} , thus, affecting g_m . Transconductance g_m is a key parameter that determines the
 157 voltage gain of the active balun, which will be discussed in the succeeding section.
 158

159 Resistors $R1$ and $R2$ could be determined given the setup for minimum attenuation and
 160 maximum voltage swing in the two outputs.
 161

$$R1 = \frac{V1}{I_{DS}} = \frac{0.2V}{I_{DS}} \quad R2 = \frac{V_{DD} - V2}{I_{DS}} = \frac{0.2V}{I_{DS}} \quad \text{Eq. (19)}$$

162

163 To have a balanced attenuation in the two outputs, R1 should be equal to R2. With V1 and
 164 V2 set to the optimum value and V_{DD} set to 1V, decreasing the supply current (which is equal
 165 to I_{DS}) would increase the value of R1 and R2. Large resistor values contribute to more
 166 noise and parasitics. Since the active balun is targeted for low power consumption, tradeoff
 167 between drain current I_{DS} and resistor values is inevitable. Moreover, the design is optimized
 168 to meet the target performance specifications suitable for WIMAX receiver. The active balun
 169 design is implemented in a standard 90nm CMOS process using Cadence Virtuoso software
 170 [6], a computer-aided design (CAD) tool and simulation software. Table 2 summarizes the
 171 common-source/drain active balun parameters.
 172

173 **Table 2. Common-source/drain active balun parameters expressions**
 174

Parameters	Value
Input bias voltage	0.8V
Output DC voltage for maximum swing	0.2V (RFout1), 0.8V (RFout2)
Input impedance	∞
Output impedance, with resistor and capacitor loads	$R1 \parallel 1/sC1$ (RFout1), $R2 \parallel 1/sC2$ (RFout2)
Voltage gain, simplified ($s = 0$)	$\frac{g_m R1}{1 + (g_m + g_{mb})R1}$ (RFout1) $\frac{-g_m R2}{1 + (g_m + g_{mb})R1}$ (RFout2)
Output noise voltage	$\frac{k_B T}{C1} [1 + \gamma(g_m + g_{mb})R1]$ (RFout1) $\frac{k_B T}{C2} [1 + \gamma(g_m + g_{mb})R2]$ (RFout2)
Noise Figure	$10 \log \left[1 + \frac{1 + \gamma(g_m + g_{mb})R1}{C1 \cdot k_B T \Delta f \cdot A_{v1}} \right]$ (RFout1) $10 \log \left[1 + \frac{1 + \gamma(g_m + g_{mb})R2}{C2 \cdot k_B T \Delta f \cdot A_{v2}} \right]$ (RFout2)

175
 176
 177
 178
 179

3. RESULTS AND DISCUSSION

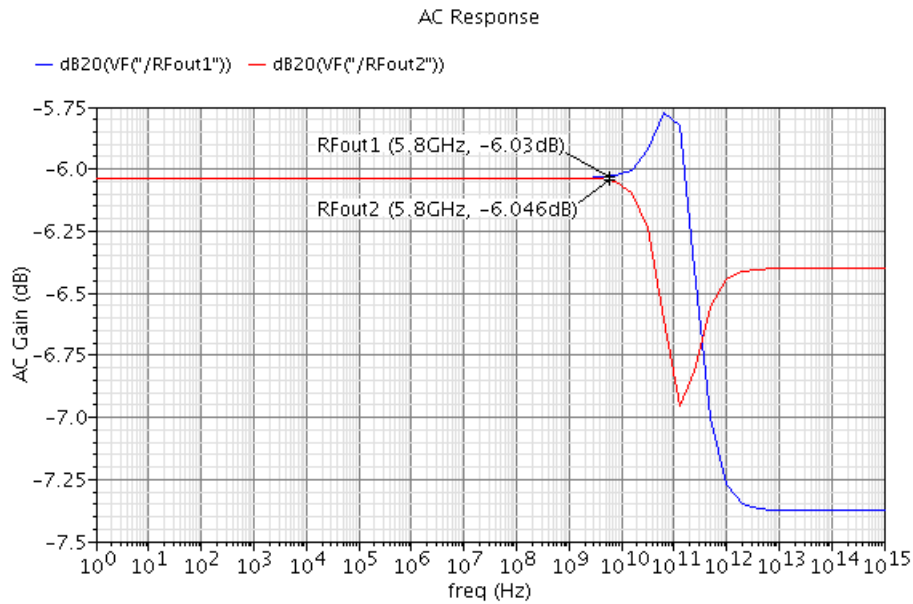
180 The common-source/drain active balun is characterized and designed to achieve the target
 181 specifications. The extraction of all device parameters for use in simulations is done using
 182 Synopsys Star-RCXT [7]. Simulations of the extracted view are done using Cadence Design
 183 Systems software. The active balun is designed to operate at 5.8GHz, which is a typical
 184 frequency for WiMAX applications. Measurements in the simulation plots are taken at
 185 5.8GHz.

186

187 3.1 Gain and Gain Difference

188

189 There are many types of power gain defined for an amplifier. The most commonly specified
190 and often the most useful is the transducer gain, G_T . It is defined as the ratio of the power
191 delivered to the load to the power available from the source. Gain difference or gain error is
192 the difference of the gains from the two output nodes of the active balun, and is considered
193 as one of the most important parameters of the active balun design. Ideally, the gain
194 difference of an active balun should be zero in magnitude. The responses in Fig. 5 and Fig.
195 6 for the gain and gain difference, respectively, are determined using AC analysis. Ideal
196 voltage source is used with input bias voltage V_{IN} set to 0.8V. Drain-to-source voltage,
197 $V_{DS,Q} = V_2 - V_1$, was measured at 528.6mV with $V_{GS} - V_t = 71.6mV$, confirming the
198 transistor M1 operating at saturation. Fig. 5 shows the response using AC analysis.



199
200
201
202

Fig. 5. AC analysis, gain plot

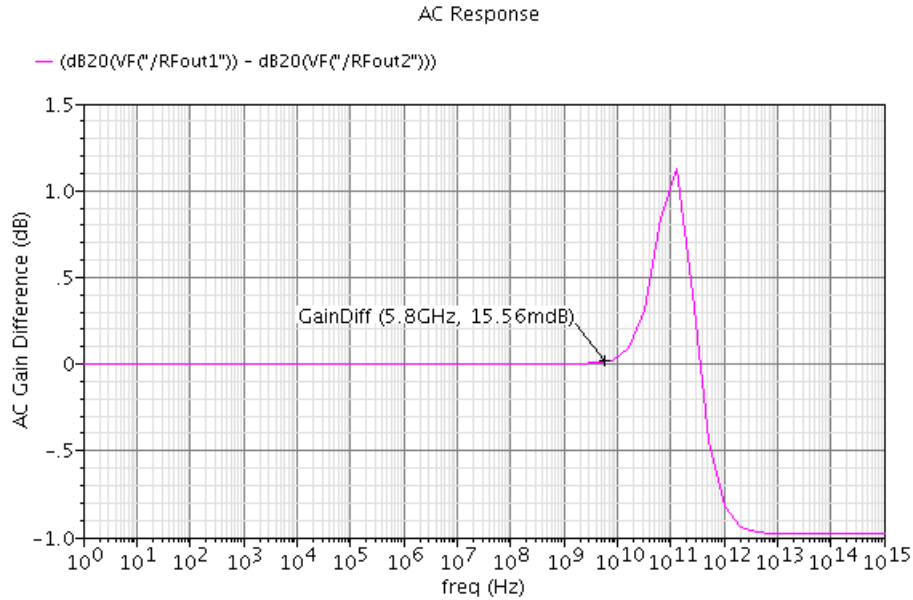


Fig. 6. AC analysis, gain difference plot

203
204
205
206
207
208
209
210
211
212
213

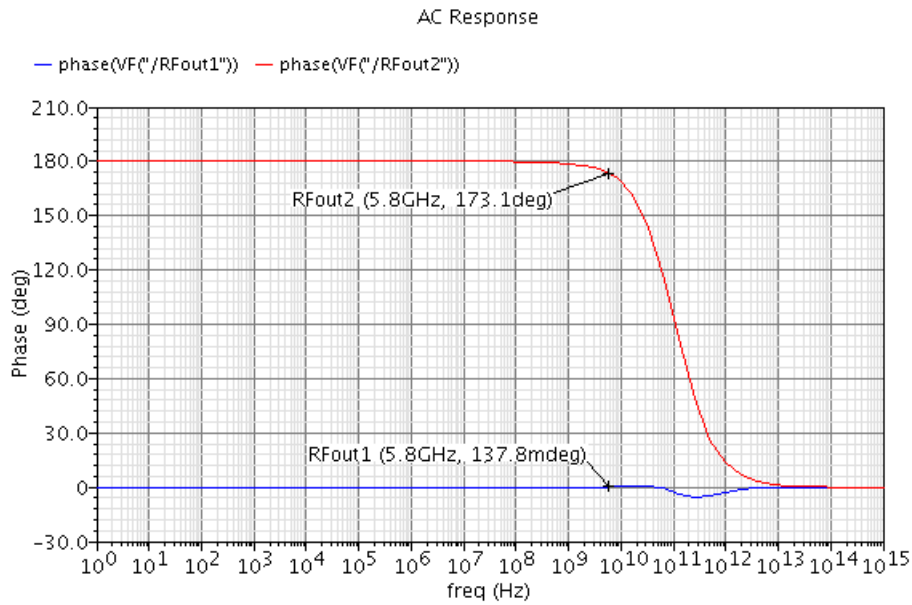
Since the active balun has the configuration of common-drain, it is expected that the gains would fall below the target of at least 0dB. AC gains are at around -6dB. Take note that the three active baluns are designed with ideal voltage source at the input, thus with very high (if not infinite) input impedance, and the output is left with no termination. Since the resistor loads of the active balun are of the same value, gain difference was maintained very low at 0.015dB.

3.2 Phase and Phase Difference

214
215
216
217
218
219

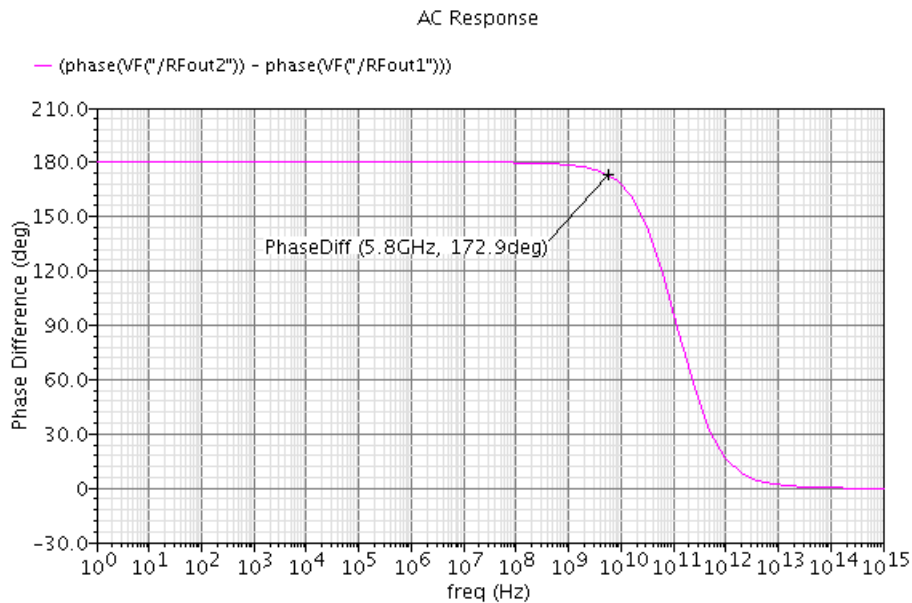
Another important parameter of an active balun is the phase difference. Phase difference is the difference between the phase of the non-inverting output node and the phase of inverting output node of the active balun. Figs. 7 and 8 show the AC analysis phase and phase difference responses, with ideal input voltage source.

220



221
222
223

Fig. 7. AC analysis, phase plot



224
225
226

Fig. 8. AC analysis, phase difference plot

227 Same analysis with the gain and gain difference are done with the phase and phase
228 difference. The results are within the acceptable values especially for the target phase
229 difference with measurement at 172.9°.

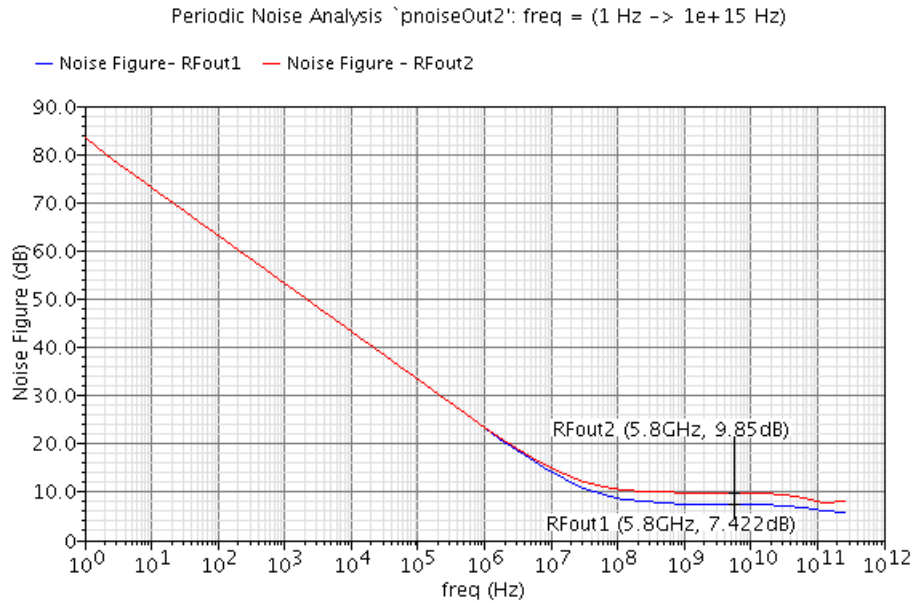
230

231 3.3 Noise Figure

232

233 Noise performance is an important design consideration since it determines the susceptibility
234 of the active balun to unwanted signal or noise. One important design parameters is the

235 noise figure (NF), which is a measure of the amount of signal-to-noise-ratio degradation
 236 introduced by the circuit as seen at the output. Fig. 9 shows the noise figure result using
 237 PSS+PNoise analysis.
 238



239
 240 **Fig. 9. Noise figure plot**
 241

242 Noise figure of 7.422dB and 9.85dB for RfOut1 and RfOut2 with respect to RFin are
 243 generated using PSS+PNoise analysis with RF input power set to -20dBm. It is worth noting
 244 that the noise figure from PNoise analysis is slightly higher than the noise figure generated
 245 from SP analysis because at prf = -20dBm the active balun demonstrated very weak
 246 nonlinearity and noise as other high harmonics are convoluted.
 247

248 **3.4 Results Summary**
 249

250 Table 3 summarizes the performance of the three active balun designs.
 251

252 **Table 3. Performance summary of differential active balun**
 253

Parameters	Target	Value
Process/Technology	90nm CMOS	90nm CMOS
Supply voltage	1V	1V
Frequency	5.8GHz	5.8GHz
Gain difference	< 1dB	0.016dB
Phase difference	180° ± 10°	172.9°
Noise figure	< 10dB	7.422dB (RfOut1), 9.850dB (RfOut2)
Power consumption	< 10mW	2.558mW

254
 255 The common-source/drain active balun design achieved a gain difference better than 1dB
 256 and a phase difference of 180°±10° or better at frequency of 5.8GHz. The balun is affected
 257 with the input and output loading since the circuit is designed with ideal input voltage source

258 and no termination ports included. Low power consumption of at most 2.56mW is achieved,
259 comparable to other low power designs in the past researches.

260
261

262 **4. CONCLUSION AND RECOMMENDATIONS**

263

264 A common-source/drain active balun is designed and implemented in a standard 90nm
265 CMOS process, and carefully designed to satisfy the WiMAX receiver requirement at
266 5.8GHz. Simulation measurements are taken for parameters such as gain, phase, gain
267 difference, phase difference, and noise figure.

268 The design achieved gain difference of less than 0.02dB and phase difference of $180^\circ \pm$
269 7.1° . Noise figure performance is at around 7.42–9.85dB, comparable to previous designs
270 and researches. Low power consumption of at most 2.56mW is achieved, comparable to
271 other low power designs.

272 Future work could include designing active balun with high gain. Although it will sacrifice the
273 bandwidth, it can still be realized at lower frequencies for practical applications. One
274 possible work would be to integrate the active balun functionality on the circuit design of a
275 differential circuit like that of the double-balanced mixer or differential LNA.

276
277

278

279 **COMPETING INTERESTS DISCLAIMER:**

280

281 Authors have declared that no competing interests exist. The products used for this
282 research are commonly and predominantly use products in our area of research and
283 country. There is absolutely no conflict of interest between the authors and
284 producers of the products because we do not intend to use these products as an
285 avenue for any litigation but for the advancement of knowledge. Also, the research
286 was not funded by the producing company rather it was funded by personal efforts
287 of the authors.

288

289

290 **REFERENCES**

291

292 1. Crols J, Donnay S, Steyaert M, Gielen G. A high-level design and optimization tool for
293 analog RF receiver front-ends. International Computer-Aided Design Conference, pp.
294 550-553; November 1995.

295 2. Gomez FR, De Leon MT, Roque CR. Active balun circuits for WiMAX receiver front-end.
296 TENCON 2010 – IEEE Region 10 Conference, pp. 1156-1161; November 2010.

297 3. Azevedo F, Fortes F, Rosario MJ. A new on-chip CMOS active balun integrated with
298 LNA. 14th IEEE International Conference on Electronics, Circuits and Systems, pp.
299 1213–1216; December 2007.

300 4. IEEE standard 802.16e-2005. Part 16: Air interface for fixed and mobile broadband
301 wireless access systems, Amendment 2: Physical and medium access control layers for
302 combined fixed and mobile operation in licensed bands, and Corrigendum 1. IEEE
303 Computer Society and IEEE Microwave Theory and Techniques Society; 28 February
304 2006.

305 5. Yang HYD, Castaneda JA. Design and analysis of on-chip symmetric parallel-plate
306 coupled-line balun for silicon RF integrated circuits. IEEE Radio Frequency Integrated
307 Circuits Symposium, pp. 527-530; June 2003.

- 308 6. Cadence Design Systems, Inc. Custom IC / analog / RF design – circuit design.
309 [https://www.cadence.com/content/cadence-www/global/en_US/home/tools/custom-ic-](https://www.cadence.com/content/cadence-www/global/en_US/home/tools/custom-ic-analog-rf-design/circuit-design.html)
310 [analog-rf-design/circuit-design.html](https://www.cadence.com/content/cadence-www/global/en_US/home/tools/custom-ic-analog-rf-design/circuit-design.html)
311 7. Synopsys, Inc. StarRC – parasitic extraction. [https://www.synopsys.com/](https://www.synopsys.com/implementation-and-signoff/signoff/starrc.html)
312 [implementation-and-signoff/signoff /starrc.html](https://www.synopsys.com/implementation-and-signoff/signoff/starrc.html)
313

UNDER PEER REVIEW