Specialized Singulation Punch Design for Package Chip-out Elimination

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ABSTRACT

In the semiconductor manufacturing industry, package chip-out is a common defect frequently encountered in trim and form (T/F) process. For thin shrink small outline package (TSSOP), top defect incurred during assembly manufacturing was the package chip-out located at the top surface of the package. In this scenario, the end-of-line (EOL) process parts per million (PPM) and its non-conformance report (NCR) are high. This paper discussed how the TSSOP20 package (hereinafter referred to as Device A) chip-out was addressed and replicated or simulated through package design simulation.

Keywords: Singulation; singulation punch; package chip-out

1. INTRODUCTION

Package chip-out is a common defect frequently encountered in trim and form (T/F) process at the semiconductor assembly manufacturing. Package chip-out is defined as a region of material missing from a body. This region does not progress completely through the component and is formed after the component is manufactured. The body is given by its length, width, and depth from a projection of the design plat-form. Through this definition, Figs. 1 and 2 show the location the signature of chip-out on the top surface of the thin shrink small outline package 20-lead (TSSOP20, hereinafter referred to as Device A) package.

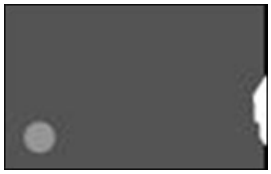

Fig. 1. Chip-out location at the lower right of the package (signature 1)

Fig. 2. Chip-out location at the upper left of the package (signature 2)

These package chip-out signatures were captured during the singulation stage at the trim and form process. Fig. 3 illustrates the assembly process flow, while Fig. 4 shows the

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process mapping of the chip-out. It is worth noting that process flow varies with the product and the technology [1-3]. With the continuing technology trends [4-7], challenges in assembly manufacturing are inevitable.

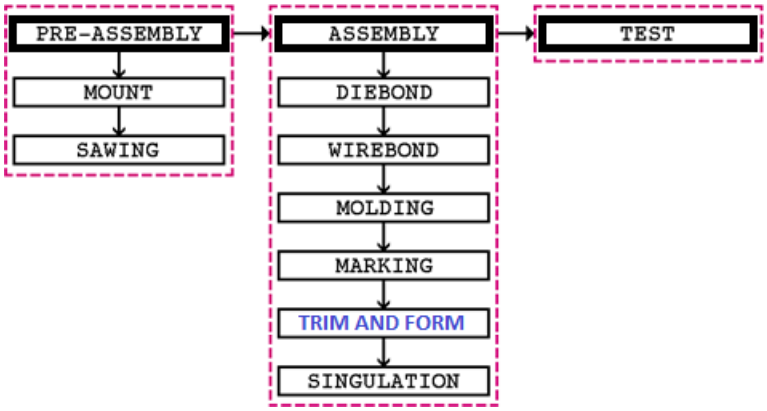

Fig. 4. Assembly process flow of Device A

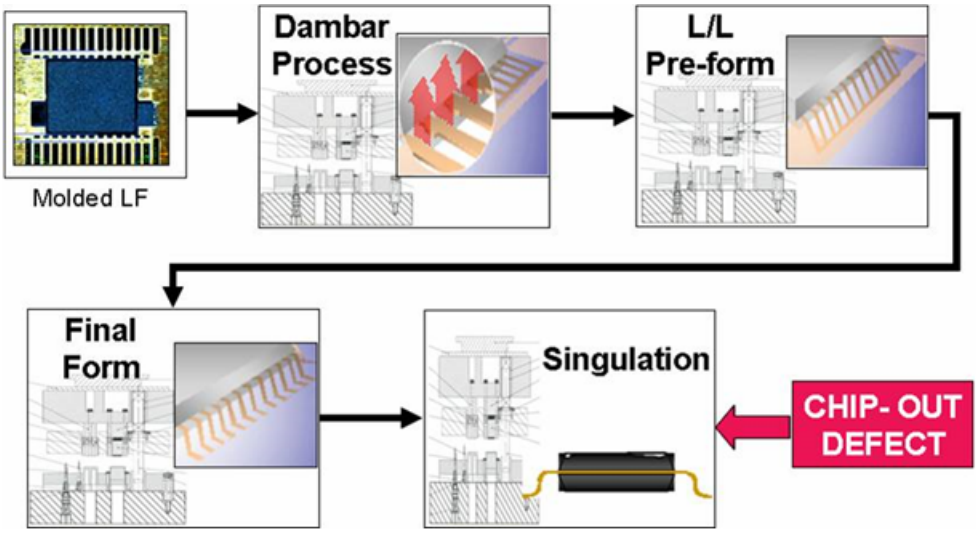

Fig. 4. Chip-out process mapping

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Fig. 5 shows how the package contacted with the tool during the singulation stage.

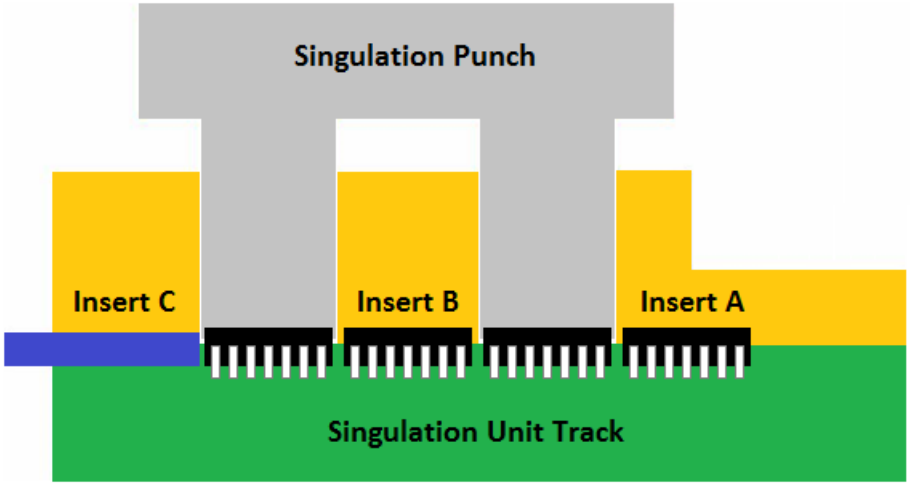

Fig. 5. Trim and form tooling for package singulation

1.1 The End-of-Line Assembly Manufacturing Performances

Device A package chip-out trend in Fig. 6 showed significant failure from January to September of 2007, for end-of-line (EOL) assembly processes.

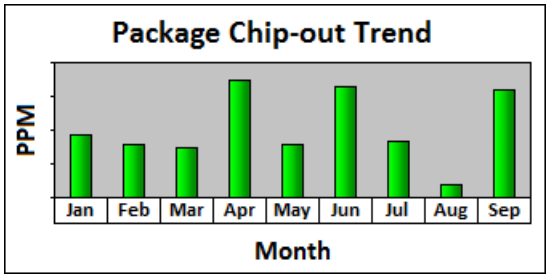

Fig. 6. Package chip-out PPM trend (actual PPM intentionally not shown)

2. EXPERIMENTAL SECTION

A dimensional analysis using the AutoCAD software [8] in Fig. 7, was performed to validate the original setup of the singulation tool. Figure 6 shows the dimensional condition of the original setup against the simulated dimensional punch requirement. It also shows the possibility of package contact clearances in case the punch will shift in the extreme left and right locations.

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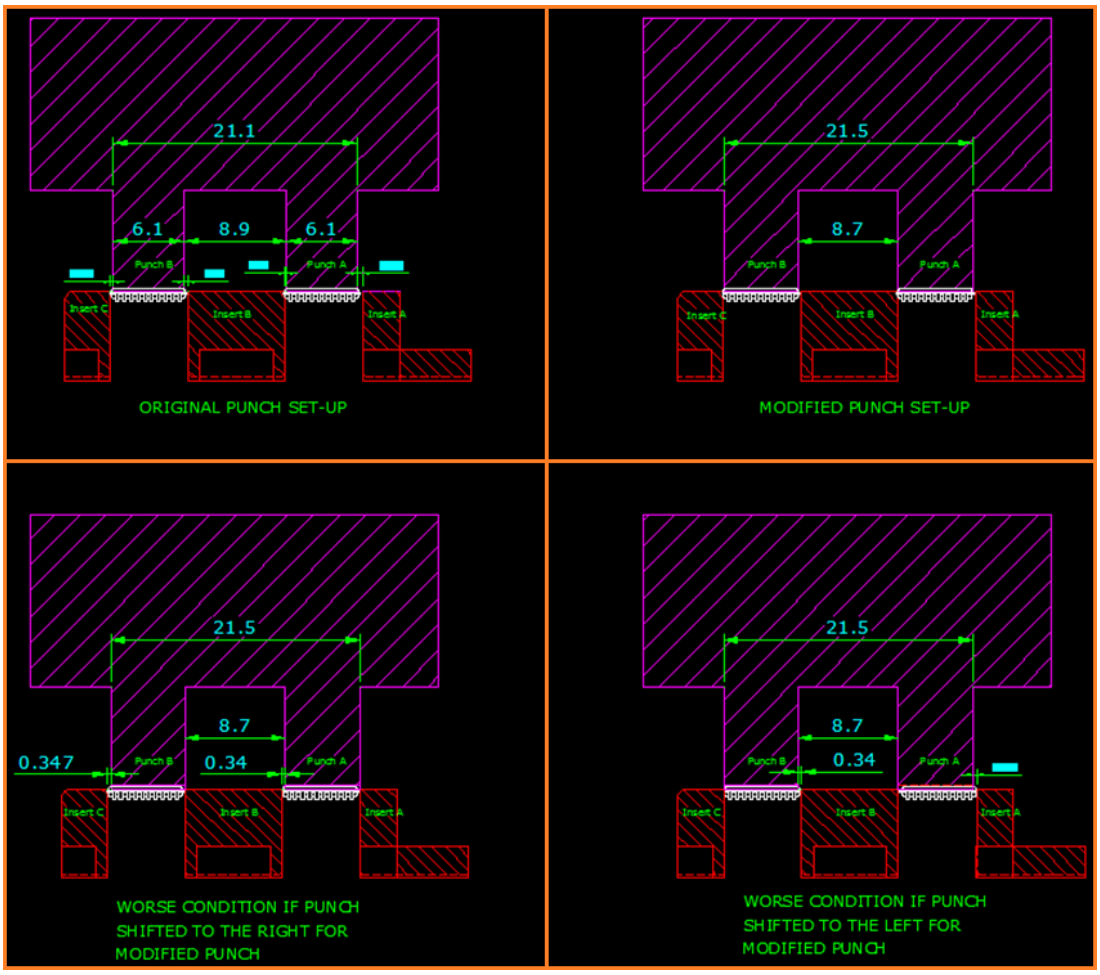

Fig. 7. Simulation with the original setup dimension condition and the required punch dimension

A package chip-out can occur in two possible situations: one at the singulation stage of trim form process in which the package has a direct contact with the singulation punch, and two at the singulation tool set-up that requires dimensional standards.

2.1 Package Chip-out Failure Mechanism on Singulation Punch

The singulation punch in TF process guides and holds the package units to singulate from the leadframe matrix. Punch applies a certain external force to the package and holds the unit to singulate. Punch requires a critical dimension in order to perform its required function. Fig. 8 shows the how the unit is being singulated in case the singulation punch does not comply with the required dimension.

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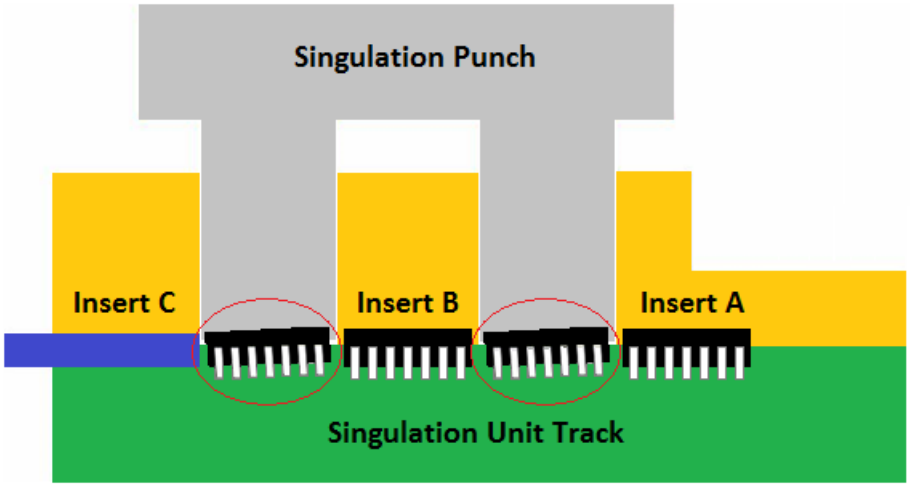

Fig. 8. Possible mis-alignment during package singulation

3. RESULTS AND ANALYSIS

3.1 Replication and Simulation of Package Chip-out Signatures

Actual validation was made based on the dimensions simulated from AutoCAD in Fig. 7. The original setup dimensions were simulated in the worst punch location condition to replicate the package chip-out signatures 1 and 2 illustrated from Figs. 1-2.

3.1.1 Package Chip-out Signature 1

Simulation and tool adjustment was made under worst condition. Fig. 9 shows the maximum shifting of package to the rightmost side of the singulation punch. This resulted to the loss of support on the top package area when there is maximum shifting of package against insert position. Based on this condition the chip-out signature 1 was replicated.

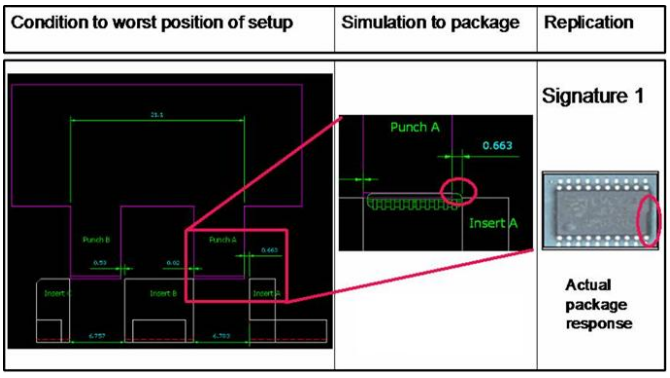

Fig. 9. Simulation and replication of chip-out signature 1

3.1.2 Package Chip-out Signature 2

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The same procedure was made to determine condition of the package chip-out signature 2. Fig. 10 shows the maximum shift of package to the left most of the singulation punch.

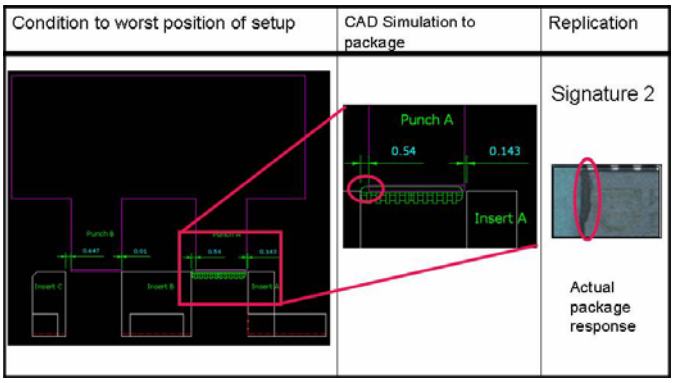
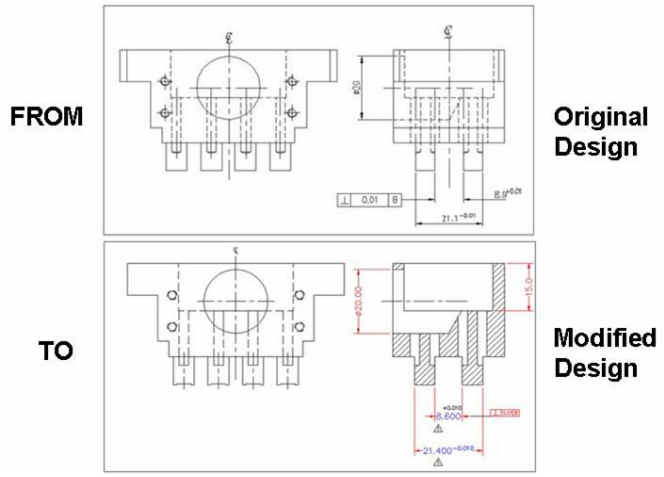


Fig. 10. Simulation and replication of chip-out signature 2

3.2 Singulation Punch Modification for Signature 1 and 2

The peripheral dimensions of the singulation punch design were modified based on the simulation and replication of the package signature chip-out. Fig. 11 shows the modified punch dimension and the 3D modeling illustration of the complete modified punch configuration to eliminate the package chip-out.



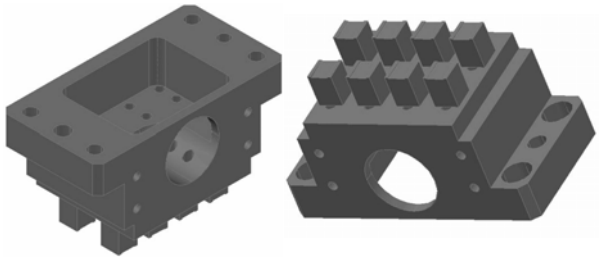


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Fig. 11. Singulation punch design modification and 3D modeling using AutoCAD software

Further data was made on a larger scale and Comparative Tests were used to statistically validate the results, with the aid of SAS-JMP [9], a system software for statistical analysis. Tukey-Kramer test was used for it gives a more conservative estimate of results as compared to the other tests. Statistical graphs are provided for ease of interpretation and analysis.

3.3 Assembly EOL Package Chip-out PPM Trend

Based on assembly EOL Device A PPM data in Fig. 12, the simulation/replication made via design modification and singulation tool clearance standardization contribute a significant improvement for eliminating package chip-out.

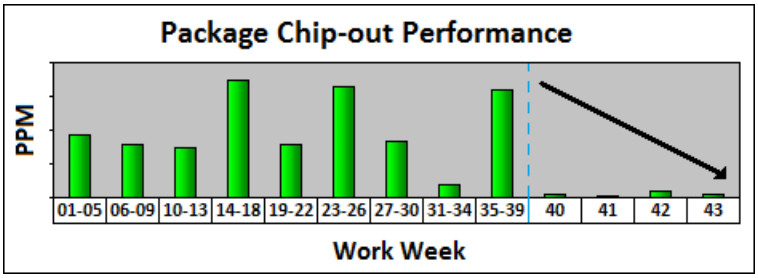

Fig. 12. Package chip-out PPM trend improvement (actual PPM intentionally not shown)

4. CONCLUSION AND RECOMMENDATIONS

The original equipment manufacturer (OEM) design for Device A singulation tool did not met the required dimensions of singulation punch for worst conditions (maximum shifting of package to meet the required clearance to support the package during singulation). The modified punch dimension significantly contributed to improve the Device A chip-out reduction for chip-out signatures 1 & 2. The most significant factor is the parts consumable replacement based on the wear and tear life condition set, this the pro-active way to maintain the best quality and performance of the singulation tool.

It is recommended that these corrective actions be sustained by understanding the wear and tear of the material via tool life identification for frequent parts replacements and maintenance. Another thing to consider is the tool clearance dimensional set-up that can be attained by an appropriate die-setting dimensional inspection. It is also important that the assembly manufacturing processes ensure proper electrostatic discharge (ESD) checks and controls. Discussions presented in [10] are helpful to realize ESD-related controls.

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