	Original Research Article
	A Study of Wafer Backgrinding Tape Selection for SOI Wafers
ABSTRACT	

The development on thinner packages has become the trend and focus in semiconductor packaging industry. The necessity of thinner packages also entails a thinner vertical structure of the integrated circuit (IC) design. As a major contributor on the vertical structure of the IC package, die or wafer is also essential to go thinner. As the wafer goes thinner, various problems may occur during transport and even the backgrinding process, itself.

Wafer warpage is one of the main concerns during the backgrinding process. Wafer warpage varies depending on the wafer backgrinding stress and BG tape tension. Hence, tension between the surface protective tape and the wafer should be considered an important and critical item to consider during BG tape selection.

Different silicon wafer technology has been released to cater different functionality on different industry markets. One popular silicon technology is Silicon On Insulator (SOI) technology. SOI wafers have a step type passivation wherein the edge of the wafer is observed to have 30um thinner than its center. The stepping effect also contributes to the 0.5mm wafer warpage prior backgrinding. Evaluating the effect of BG tape selection to eliminate such warpage is discussed on this paper.

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Keywords: Silicon on insulator; backgrinding tape; wafer preparation; SOI wafer.

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14 1. INTRODUCTION

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Achieving the package requirements of an integrated circuit (IC) semiconductor device would mean attaining a thinner die during the back end process. The major process brick responsible for grinding the silicon die to its thickness is wafer backgrinding. As a major preliminary process at the back end, one of its sub-processes is the wafer preparation prior grinding wherein silicon wafer is been taped on the active layer to protect it from any contaminants and water penetration during the grinding process.

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One major factor for wafer warpage after grinding is the wafer backgrinding tape (hereinafter referred to as BG tape). The adhesion strength of the BG tape will induce the amount of wafer warpage and edge chipping of the grinded wafer. The study focuses on the effect of different BG tapes that can handle wafer warpage.

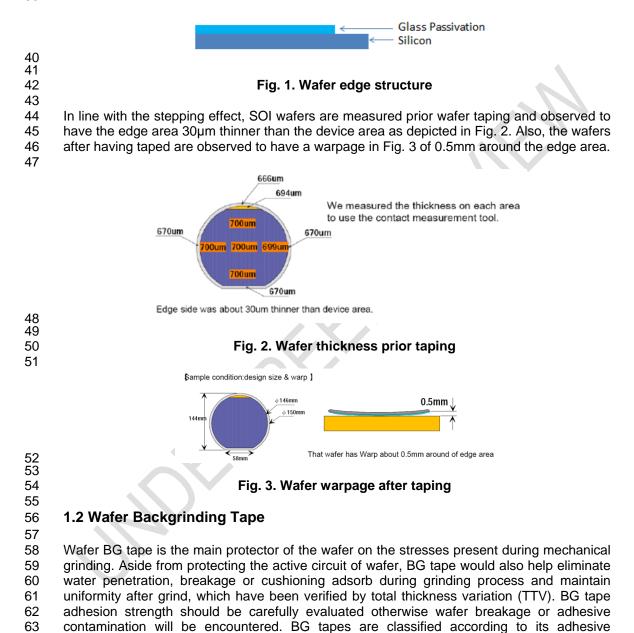
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1.1 Silicon On Insulator Wafer

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Silicon on insulator (SOI) wafer technology refers to the use of a layered silicon-insulator silicon substrate, to reduce parasitic capacitance and thereby improving performance [1].
 The implementation of SOI technology is one of several manufacturing strategies employed
 to allow the continued miniaturization of microelectronics colloquially referred to as extending

Moore's Law [2]. SOI process has been developed so as to be used for RF applications. The inclusion of enhanced sapphire substrate allows the complementary metal-oxide semiconductor (CMOS) node to have a high isolation, high linearity, and electrostatic discharge (ESD) tolerance. The glass passivation on the wafer's top layer creates a stepping effect on the edge of the wafer in Fig. 1.



- 64 material; the two types of BG tape are: Conventional non-ultraviolet (non-UV) type and UV 65 curable type.
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Due to inherent wafer warpage of the SOI wafers, the two different types have been used to
 check if it helps adsorb the grinding stress and prevent wafer breakage during

grinding/detaping process. Both BG tape have almost the same tape thickness of 124 125µm, but different on the adhesive material used.

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2. LITERATURE REVIEW

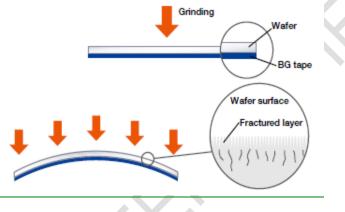
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2.1 Wafer Warpage Mechanism

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A common wafer mechanism is a normal warpage [3] illustrated in Fig. 4. This is generally caused by the natural stress created by mechanical backgrinding. The proportional relationship of wafer warpage and mechanical stress states that when the final thickness decrease this probably caused by high mechanical stress that may lead to high wafer warpage.

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Fig. 4. Normal warpage

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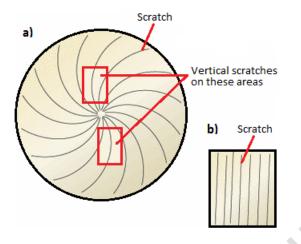
86 2.2 Mechanical Stress After Wafer Backgrinding

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Stresses applied during encapsulation may crack the die and cause other stress-related failures. Optimized wafer strength is needed to ensure reliability during both fabrication and packaging. However, grinding anything inevitably leaves flaws on its surface, which can weaken both the wafer and the individual dice sawn from it. Given thermal or mechanical stress, these flaws may then spread into active regions, and may crack the die.

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After backgrinding, the wafer will exhibit a scratch pattern on the backside as shown in Fig. 5. These scratch patterns and the depth of the scratches on the surface of the wafer are directly proportional to the size of the grit and the pressure exerted on the wafer during the grinding process. The depth of the scratches and the backside surface roughness of the semiconductor die have a direct correlation to the strength of the die, so it is critical that the finished backside surface of the wafer be as smooth (or polished) as possible [4].



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Fig. 5. Vertical scratches after wafer backgrinding

104105 3. EXPERIMENTATION

107 3.1 BG Tape Selection

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109 One major factor that could help minimize the wafer warpage is the BG tape. Proper 110 selection of the BG tape involves the study of the adhesion strength of the tape towards the 111 wafer during wafer back grinding thus inducing a much more wafer warpage after 112 backgrinding.

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Two different BG tapes in Table 1 have been evaluated to help reduce the wafer warpage prior and after wafer back grinding. Both tapes are on almost the same thickness, 125µm and 120µm respectively. Conventional tape is observed to have lowered adhesion strength before UV compare to UV tape BG tapes. However, UV types improves to 0.1N/25mm after UV exposure that could possibly help lessen the stress of the BG tape during the detaping issue thus reducing wafer warpage. Wafer warpage and wafer edge chipping will depend on the effectiveness of the BG tape.

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Table 1. BG tape configuration

Specification	Unit	Conventional	UV Tape
Total thickness	μm	125	120
Adhesive thickne	ss µm	20	40
Be Adhesion strength	fore UV N/25mi	2.84	6.5
Ũ	fter UV	2.04	0.1

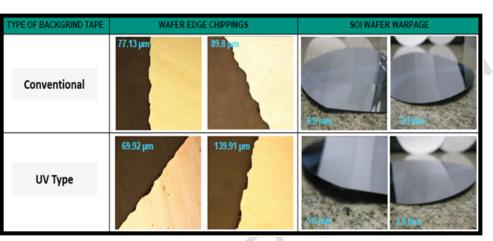
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126 4. RESULTS AND DISCUSSION

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Both BG tapes in Fig. 6 induced wafer edge chippings and wafer warpage. The amount of wafer warpage for both BG tapes shows comparable level after backgrinding. Wafer edge chippings are observed being similar for both BG tapes. The readings of both tapes showed potential cause of wafer breakage. Both BG tapes have not been successful to be processed using the full auto mode due to its high warpage during the unloading. The robot arm vacuum is not enough to handle even the minimum warpage of 3.0mm.

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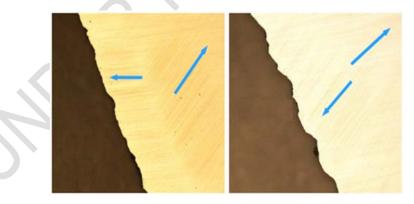


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Fig. 6. Wafer edge chipping and wafer warpage after backgrinding

Back side image of the wafer has also been inspected using high magnification microscope as shown in Fig. 7. Uneven surface was observed at the edge of the wafer, which can also be considered a potential cause of broken wafer during process of transporting wafer from one station to another at pre-assembly. Also, the occurrence of uneven surface at the back of the wafer also coincide with the step at the edge of the wafers.



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Fig. 7. Back side image of the SOI wafer

149 5. CONCLUSION AND RECOMMENDATIONS

Adhesion strength of the BG tape was negated by normal warpage phenomena on the wafer. The BG tape, even on UV type tapes, could not equalize the amount of mechanical stress on the wafer surface structure thus increasing the effect of wafer warpage towards the silicon wafer. Both BG tape also could not negate the step type structure of the wafer thus
 creating wafer edge chippings and could be resulting wafer warpage if not fully controlled
 during handling.

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158 For added improvement, it is highly recommended to use high vacuum efficient chuck table 159 to properly handle incoming wafer warpage and ensure good flattening on the chuck table and eliminating the possibility of inferior grinding. Redesign of special robot arms should also 160 be considered to eliminate the possibility of wafer breakage when handling or unloading 161 162 thinner wafers after grinding or use an inline BG-mount system. Moreover, a special process should be considered wherein making an outer circumference lip, where no grinding 163 pressure is applied on the edge of the wafer during backgrinding. It is also important that the 164 assembly manufacturing processes ensure proper ESD checks and controls. Discussions 165 presented in [5] are helpful to establish proper ESD-related controls. 166

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